

Material	Stack-Up	Vias	Parameter	Layer
Plating	25µm			LY-Top SIG
Copper	17µm			
NP-155fb	50µm		100-150-100µm d 100 Ω	150µm s 50 Ω
NP-155fb	50µm			
Copper	17µm		1V8 1V2	LY-2 GND
NP-155ftl	50µm			
Copper	17µm			LY-3 VCC
NP-155fb	65µm		4.7µF 1.5nF 4.7µF 10nF	
NP-155fb	65µm			LY-4 SIG
Copper	17µm		100-150-100µm d 100 Ω	150µm s 50 Ω
NP-155ftl 600µm				
DRth 1-8				
Copper	17µm		100-150-100µm d 100 Ω	150µm s 50 Ω
NP-155fb	65µm			LY-5 SIG
NP-155fb	65µm		4.7µF 150nF	
Copper	17µm			LY-6 VCC
NP-155ftl	50µm			
Copper	17µm		3V3	LY-7 GND
NP-155fb	50µm			
NP-155fb	50µm		100-150-100µm d 100 Ω	150µm s 50 Ω
Copper	17µm			
Plating	25µm			LY-Bot SIG

Thickness 1.16mm - 1.42mm Bare Board
 1.24mm - 1.51mm ENIG
 1.27mm - 1.55mm HAL
 General tolerance +,- 6%

LA-Drawing #1024
 Date 11.06.2010 / 16.11.2010 Wi
 Name Wi
 Comment --

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RST1-40C50-17C600-17#01

Material	Stack-Up	Vias	Parameter	Layer
Ptiring	25µm			L>Top SHI
NP-155B	50µm 106 SR-70		100±10, 100±10 @ 100.0	150µm ± 0.0
NP-155B	50µm 106 SR-70		I/V-B + I/V-2	L-V-2 GND
NP-155B	17µm 50µm			L-V-3 VCC
NP-155B	17µm 50µm			L-V-4 SHI
Copper	17µm			
NP-155B	650µm			
NP-155B	650µm 1000 MR-67		100±10, 100±10 @ 100.0	150µm ± 0.0
Copper	17µm			
NP-155B	650µm 1000 MR-67		I/V-5	L-V-5 SHI
NP-155B	650µm 1000 MR-67		I/V-6	L-V-6 VCC
Copper	17µm			
NP-155B	50µm 106 SR-70		I/V-3 -4	L-V-7 GND
NP-155B	50µm 106 SR-70		100±10, 100±10 @ 100.0	150µm ± 0.0
Copper	17µm			
NP-155B	25µm			L-V-Bot SHI

Thickness : 1.58mm ± 1.42mm Bare Board
 1.24mm ± 1.21mm ENIG
 1.27mm ± 1.55mm HAL
 Gerberstandard v4x

LA-Drawing #1024
 Date 11.08.2010
 Name VM
 Comment

IPC-Specification sheet	IPC-4101C / 99
Epoxy-System	FR4
Curing agent	phenolic
Flame retardend mech.	RoHS compliant Bromine
UL-zertificate	UL94 V-0
Dielectric value	4.1@1GHz
Loss tangent	0.014@1GHz
Tg	150° by DSC
CTE x/y/z	before Tg : 18/18/ maximum 60 after Tg : 18/18/ maximum 300
Electrical strength	40 kv/mm minimum specified by IPC
Adhesive strength	0.78 n/mm minimum for copper foils >17µm

[illegible]

PCB Class	Rigid
Cores mounted	Inside
Copper Thickness	25µm for throughhole barrels
Throughhole Vias	CAD : 100µm diameter + 400µm pad minimum Tool : 200µm diameter minimum
Aspect-Ratio	1:8 or better is necessary
BuriedVias	no
BlindVias	no
Track width	100µm minimum on all signal layers
Track distance	90µm minimum on all signal layers
Solder Mask	double sided, fotolithographic, thickness 20µm
Plugging	no
Edge Metallisation	no
UL	yes

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Decoupling Capacitors are calculated with DCC Silent V.4.0

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Tool diameter 200 μ m