Extension	Meaning	Additional Information
Unprivileged Architecture		
Base		
RVWMO	Weak memory ordering	
RV32I	Base Integer Instruction Set, 32-bit	
RV32E	Base Integer Instruction Set for microcontrollers, 32-bit	
RV64I	Base Integer Instruction Set, 64-bit	
RV64E	Base Integer Instruction Set for microcontrollers, 64-bit	
Extension		
Zifencei	Instruction-Fetch Fence	
Zicsr	Control and Status Register (CSR) Instructions	
Zicntr	Base Counters and Timers	
Zihpm	Hardware Performance Counters	
Zihintntl	Non-Temporal Locality Hints	
Zihintpause	Pause Hint	
Zimop	May-Be-Operations	
Zcmop	Compressed May-Be-Operations	
Zicond	Integer Conditional Operations	
M	Integer Multiplication and Division	
Zmmul	Multiplication subset of the M extension	
A	Atomic Instructions	
Zalrsc	Load-Reserved/Store-Conditional Instructions	
Zaamo	Atomic Memory Operations	
Zawrs	Wait-on-Reservation-Set Instructions	
Zacas	Atomic Compare-and-Swap (CAS) Instructions	
Zabha	Byte and Halfword Atomic Memory Operations	
Ztso	Total Store Ordering	
CMO	Tbase Cache Management Operation ISA	
Zicbom	Cache-Block Management Instructions	
Zicboz	Cache-Block Zero Instruction	

Zicbop	Cache-Block Prefetch instructions	
F	Single-Precision Floating-Point	
D	Double-Precision Floating-Point	
Q	Quad-Precision Floating-Point	
Zfh	Half-Precision Floating-Point	
Zfhmin	Minimal Half-Precision Floating-Point	
BF16	BFloat16-precision Floating-Point	
Zfbfmin	Scalar BF16 Converts	
Zvfbfmin	Vector BF16 Converts	
Zvfbfwma	Vector BF16 widening mul-add	
Zfa	Additional Floating-Point Instructions	
Zfinx	Single-Precision Floating-Point in Integer Register	
Zdinx	Double-Precision Floating-Point in Integer Register	
Zhinx	Half-Precision Floating-Point in Integer Register	
Zhinxmin	Minimal Half-Precision Floating-Point in Integer Register	
C	Standard Extension for Compressed Instructions	
Zca	Refers to Instruction in C extension that do not include the floating-point loads and stores	C always implies Zca
Zcf	Refers to compressed single-precision floating-point load/stores	C+F implies Zcf (RV32 only)
Zcd	Refers to compressed double-precission floating-point load/stores	C+D implies Zcd
Zcb	Simple operations for use on all architectures	
Zcmp	PUSH/POP and double move Instructions. Complex operations intended for embedded CPUs	
Zcmt	Table jump Instructions. Complex operations intended for embedded CPUs	
Zce	Intended to be used for microcontrollers, includes all relevant Zc* extensions	On RV32: with F implies: Zca, Zcb, Zcmp, Zcmt, Zcf without F implies: Zca, Zcb, Zcmp, Zcmt On RV64: Zca, Zcb, Zcmp, Zcmt
B	Standard Extension for Bit Manipulation	Implies Zba, Zbb and Zbs
Zba	Address generation Instructions	
Zbb	Basic bit-manipulation	

Zbc	Carry-less multiplication	
Zbs	Single-bit instructions	
Zbkb	Bit-manipulation for Cryptography	
Zbkc	Carry-less multiplication for Cryptography	
Zbkx	Crossbar permuatations for Cryptography	
V	Standard Extension for Vector Operations	for Application Processors
Zvl*b	Minimum Vector Length Standard Extensions	* is a placeholder for the length
Zve*	Vector Extensions for Embedded Processors	Support different VLEN, EEW, FP or no FP
Zve32x	Vector Instructions, 32-bit	
Zve32f	Vector floating Point Instructions, 32-bit	
Zve64x	Vector Instructions, 64-bit	
Zve64f	Vector floating Point Instructions, 64-bit	
Zve64d	Vector floating Point Instructions, 32- and 64-bit	
Zvfhmin	Vector Extension for Minimal Half-Precision Floating-Point	
Zvfh	Vector Extension for Half-Precision Floating-Point	
Zknd	NIST Suite: AES Decryption	
Zkne	NIST Suite: AES Encryption	
Zknh	NSIT Suite: Hash Function Instructions	
Zksed	ShangMi Suite: SM4 Block Cipher Instructions	
Zksh	ShangMi Suite: SM3 Hash Function Instructions	
Zkr	Entropy Source Extension	
Zkn	NIST Algorithm Suite	Implies: Zbkb, Zbkc, Zbkx, Zkne, Zknd, Zknh
Zks	ShangMi Algorithm Suite	Implies: Zbkb, Zbkc, Zbkx, Zksed, Zksh
Zk	Standardscalar cryptography extension	Implies: Zkn, Zkr, Zkt
Zkt	Data Independent Execution Latency	
Zvbb	Vector Basic Bit-manipulation	
Zvbc	Vector Carryless Multiplication	
Zvkb	Vector Cryptography Bit-manipulation	
Zvkg	Vector GCM/GMAC	
Zvkned	NIST Suite: Vector AES Block Cipher	

Zvknh[ab]	NIST Suite: Vector SHA-2 Secure Hash	Zvknha: SHA-256 and SHA-512 Zvknha: SHA-256
Zvksed	ShangMi Suite: SM4 Block Cipher Instructions	
Zvksh	ShangMi Suite: SM3 Secure Hash	
Zvkn	NIST Algorithm Suite	Implies: Zvkned, Zvknhb, Zvkb, Zvkt
Zvknc	NIST Algorithm Suite with carryless multiply	Implies: Zvkn, Zvbc
Zvkng	NIST Algorithm Suite with GCM	Implies: Zvkn, Zvkg
Zvks	ShangMi Algorithm Suite	Implies: Zvksed, Zvksh, Zvkb, Zvkt
Zvksc	ShangMi Algorithm Suite with carryless multiplication	Implies: Zvks, Zvbc
Zvksg	ShangMi Algorithm Suite with GCM	Implies: Zvks, Zvkg
Zvkt	Vector Data-Independent Execution Latency	Impies: Zvbb, Zvbc
Zicfilp	Landing Pad	
Zicfiss	Shadow Stack	
Zilsd	Load/Store pair instructions	
Zclsd	Compressed Load/Store pair instructions	
Privileged Architecture		
Smstateen	State Enable Extension	
Ssstateen	State Enable Extension, without mstateen*	
Smcsrind	Encompasses all added CSRs and all behavior modifications for a hart, over all privilege levels	
Sscsrind	Same as Smcsrind excepte excluding the machine-level CSRs and behavior not directly visible to supervisor level	
Smepmp	Extension for PMP Enhancements of memory access and execution prevention in Machine mode	
Smcntrpmf	Cycle and Instret Privilege Mode Filtering	
Smrnmi	Extension for Resumable Non-Maskable Interrupts	
Smcdeleg	Counter Delegation Extension	
Ssccfg	Counter Configuration Extension for Supervisor-level environments	
Smdbltrp	Double Trap Extension	
Smctr	Control Transfer Records Extension for all privilege levels	
Ssctr	Control Transfer Records Extension for all privilege levels but machine	
Svnapot	Extension for NAPOT Translation Contiguity	

Svpbmt	Extension for Page-Based Memory Types	
Svinval	Extension for Fine-Grained Address-Translation Cache Invalidation	
Svadu	Extension for Hardware Updating of A/D Bits	
Svvptc	Extension for Obviating Memory-Management Instructions after marking PTEs Valid	
Ssqosid	Extension for Quality-of-Service (QoS) Identifiers	
Sstc	Extension for Supervisor-mode Timer Inerrupts	
Sscofpmf	Extension for Count Overflow and Mode-Based Filtering	
H	Hypervisor Support	
Zicfilp	Landing Pad	
Zicfiss	Shadow Stack	
Ssdbltrp	Double Trap Extension	
Ssnpm	Pointer Masking Extension for U- and VU-mode	
Smnpm	Pointer Masking Extension for S- and HS-mode	
Smmpm	Pointer Masking Extension for M-mode	
Sspm	Extension that indicates that pointer-masking support is available in supervisor mode	
Supm	Extension that indicates that pointer-masking support is available in user mode	
Advanced Interrupt Architecture		
Smaia	Extension for advanced Interrupts in machine-level execution environements	
Ssaia	Extension for advanced Interrupts in supervisor-level execution environements	
RISC-V Debug Specification		
Sdext	Extension for external debugging	
Sdtrig	Extension for triggers	